

Utilising the PDSP16256 Filter Design Program
Application Note

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1.0 BACKGROUND

To help digital filter designers a program has been developed which generates the filter coefficients and allows software modeling of the filter response. This program (called the "PDSP16256 Filter Design Program") prompts designers for the system characteristics and filter design criteria, and computes the best coefficients to implement the desired filter characteristics. Unfortunately this software only works for single '256 designs and does not (directly) support multiple '256 designs using external cascading. For designers wanting a digital filter with tap length longer than that which is supported by a single device, there is no easy way to generate coefficients. This application note describes a way to use the filter design program for externally cascaded filters up to 128 taps long.

A single PDSP16256 (or PDSP16256A) FIR filter device (hereafter collectively called the '256) can be configured as a single filter, dual independent filters, or dual independent filters which are internally cascaded. For each of the configurations the maximum filter length (i.e. "taps") is determined by the ratio of the input and output sample rates to the system clock rate. The limitation is due to the fixed number of multiply/accumulate subsections in the device, and the need to multicycle them as the filter length is increased. The data sheet has tables identifying the maximum number of taps for sample rates in single filter mode (ref. Table 3, P. 126) and in dual filter mode (ref. Table 4, P. 128).

When additional tap length is required for a given input sample rate, multiple '256's may be externally cascaded together. There is no limit to the number of '256 devices which may be cascaded, although maintaining the overall numeric precision and avoiding arithmetic overflow needs to be carefully considered when cascading. To implement an external cascade of '256 devices, each device is programmed as a "single" filter (the "dual" and "cascaded" modes of operation are not supported when externally cascading).

2.0 THEORY

When executing the design program, two DOS files are generated to keep the filter characteristics, coefficients, and '256 configuration information. By editing one of the two files, it is possible to force the coefficient generating subroutines and filter output plotting routines to run with longer tap length filters than normally can be used in a single device. This technique will work up to the software limit of the compiled program, which is 128 taps.

To use the filter design program, start by typing "DESIGN" in the directory where the program was installed. As the software loads into memory, it will prompt you for a design file name (hereafter referred to as "<filename>") allowing the filter characteristics to be saved. The file name displayed is "FILTERxx" (where xx can be numbers or letters, but by default are nulls). Most designers enter their own eight (8) character DOS file name to provide some indication of what the filter characteristic is. Entering unique filenames allows previous filter simulations to be recalled, or evaluations of filter characteristic tradeoffs to be completed and compared to each other. Resulting calculations from the filter design program are stored in two external files using the specified file name, with .DSP and .COE extensions.

The <filename>.DSP file is an ASCII text file containing six data items. The first five items are the filter hardware characteristics. These are entered by the filter designer, and the values are stored on the first five lines (in the order shown below). The sixth line contains the calculated maximum number of filter taps, which is inserted by the program. The file is shown below, with available choices and the defaults:

LINE	DESCRIPTION	CHOICES	DEFAULT
Line #1	Device Type	PDSP16256 or PDSP16256A	PDSP16256
Line #2	Clock Rate (in Mhz)	Up to 20 for the PDSP16256, or up to 25 for the PDSP16256A	20 (PDSP16256) or 25 (PDSP16256A)
Line #3	Input Sample Rate	Clock rate (1,2,4,8)	Clock rate 1
Line #4	Filter mode	Single, Dual, Cascade	Single
Line #5	Decimation by 2	Off (0) or On (-1)	Off (0)
Line #6	Maximum # of taps	Calculated by program	Max. possible

Table 1.

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This file limits the number of taps in the “Edit Design Parameters” section of the filter design program. Filter designers may enter any number of taps up to and including the maximum number specified in the .DSP file, but not more. If a number in excess of the maximum allowable is entered, the software merely returns the previously displayed value. By editing the sixth line of the <filename>.DSP file to be equal to the desired number of total taps, the program can be tricked into calculating coefficients for externally cascaded configurations up to 128 taps (regardless of input sample rate and system clock rates). Coefficient information (which is stored in the <filename>.COE file) may then be extracted so the proper coefficients will be placed into the appropriate cascaded digital filter device.

3.0 IMPLEMENTATION

To design a filter using externally cascaded devices with up to 128 taps, the following steps should be taken:

1. Run the filter design program by typing “design” in the installed directory.
 2. Enter a carriage return, then a filter design file name up to eight characters long.
 3. Enter information about the clock rate, and input sample rate. Specify the filter mode to be “single”. Select whether decimation is desired or not.
 4. Select “Main Menu” then “Quit” to exit the program.
 5. Use an editor to edit the resulting <filename>.DSP file (which the program generated). Change the last line of the file to be the number of taps you would like to have, up to and including 128.
 6. Restart the filter design program by typing “design” again.
 7. Enter a carriage return, then enter the file name of the file you just edited.
 8. Select the “Filter Design” option, then the “Design Filter” option.
 9. Enter the filter type (lowpass, highpass, bandpass, bandstop, hilbert transform, or delay).
 10. Edit the “frequency template” information. Remember that the cutoffs are expressed as a percentage of F_s .
 11. Select “Edit Design Parameters”, and select which of the design parameters the software should calculate. This is called the “free parameter”.
 12. Specify the remaining filter design parameters.
 13. Select “Calculate Coefficients” to generate the coefficients.
 14. It may require several iterations of steps 10 - 13 to generate coefficients. If the software indicates it’s “Unable to generate coefficients” the specifications desired are too severe for the specified number of filter taps. Either simplify the filter parameters, or increase the number of taps (using the technique presented here) up to a maximum of 128, and try again.
15. After coefficients have been generated, spectral response can be viewed by selecting the “Plot Response” button on the screen. Frequency domain, impulse response, and step response graphs are the options.

When the filter characteristics desired have been achieved, exit the program and edit the <filename>.COE file. In this file, the design parameters and coefficients are stored. The format for this file is as follows:

- Line #1 - Filter type, represented by number as indicated below:
 0. Delay
 1. Lowpass
 2. Highpass
 3. Bandpass
 4. Bandstop
 5. Hilbert Transform
- Line #2 - Cutoff frequencies 1 & 2, expressed as a percentage of F_s .
- Line #3 - Four values separated by spaces (20h), indicating the following (in order below):
 1. # of filter taps used in solution (up to 128 max.)
 2. Transition width.
 3. Pass band ripple.
 4. Stopband attenuation.
- Line #4 - Coefficients, starting with the first, separated by spaces (20h).
- Lines #5 to #8 - Place holders for similar information when doing dual filter designs. Do not alter the information (mostly zeros) in these lines when doing an externally cascaded filter design.

The coefficients to be used will be found on the fourth line, separated by spaces (20h). These coefficients may then be manually partitioned into the ‘256 devices in your design to achieve the overall filter characteristic at the desired input sample rates.

4.0 EXAMPLE

We want to digitally process the information which is modulated onto the color subcarrier frequency used in NTSC televisions. Our application requires processing of the luminance information. We are not particularly concerned about processing the chroma signal, for it is being handled by a separate chroma circuit. To do the luma processing we need to extract 400 Khz of the color subcarrier, centered at 3.58 Mhz. The input has been sampled previously at 14.3 Mhz, and the 14.3 Mhz clock is available. The filter design criteria are as follows:

- System clock rate of 14.3 Mhz
- Input sample rate of 14.3 Msamples / second.
- A bandpass filter is to be developed, with the following design criteria:
 1. Pass band center frequency of 3.58 Mhz (color subcarrier frequency).
 2. Bandpass width of 400 Khz (desired bandwidth of modulated data).
 3. Stopband attenuation of -50 dB or better.

4. 100 milli dB of pass band ripple.
5. 1.3 Mhz transition width (maximum)

With the 400 Khz bandwidth desired, the values for cutoff frequency #1 and cutoff frequency #2 can be determined to be 3.58 Mhz \pm 200 Khz. This gives us 3.38 Mhz for cutoff #1, and 3.78 Mhz for cutoff #2. To avoid aliasing the input sampling rate should exceed the highest frequency signal present by a factor of 2. With cutoff #2 at 3.78 Mhz, that means the Nyquist sampling rate must be greater than 7.56 Mhz. Options for setting up the '256 device include specifying the input sample rate equal to the system clock rate, or divided by 2, 4 or 8. The only option to avoid aliasing will be to design the system to use the '256 in a non-decimating, input sample equal to the system clock configuration.

To get the stopband attenuation, pass band ripple and 400 Khz pass band width will require more than 16 taps, which is the limit using a single '256 device. To determine the total tap length required of our digital filter we can experiment with the filter design program. We begin by executing steps 1-10 in the listing above (for step #5 pick 128, for step #9 choose "Bandpass", for step #10 put the 2nd cutoff frequency at .264 and the 1st cutoff frequency at .236). You'll notice (after pressing <esc>) that the picture of the filter frequency response at the top left of the screen changes to a narrow bandpass. At step #11, allow the "Transition Width" to be the free parameter. Specify 128 for the # of taps, 100 for the pass band ripple, and -50 for the stopband attenuation. Selecting "Generate coefficients" will now produce a set of coefficients for a 128 tap filter. To determine how many taps are actually required to implement this function, return to the "Design Filter" section, and begin reducing the number of taps. When the tap length is reduced below the amount required, the software will be unable to generate the coefficients. Multiple passes through the program will prove 78 taps are required.

In single filter mode with sample clock equal to system clock and no decimation the maximum number of taps achievable in a single device is 16. For a 78 tap filter, 5 cascaded devices would be required (i.e. $\text{int}((78 / 16) + 1)$). To associate the generated coefficients with the appropriate '256 device, edit the <filename>.coe file, and extract coefficients from the fourth line, modulo 16. The first '256 device would receive the first 16 coefficients (C00 - C15), the second would receive the next 16 coefficients (C16-C31), and so forth until the fifth device, which receives the last 16 coefficients (C64 - C79). The last two coefficients (C78, C79) will be zeros.

Assuming the program constraints are such that the purchase of five '256's to implement the filter function is not plausible, consider some things which might be done to simplify the hardware:

- Relaxation of the filter design specifications. The 400 Khz pass band width is narrow, and coupled with the pass band ripple specification of 100 milli-dB make this a difficult filter to implement.
- Raising the input sample rate and system clock rate so the upper frequency transition is not so close to the Nyquist limit would help.

- The pass band of the filter is much lower in frequency than the input sample rate, it would be nice to be able to decimate the filter output, allowing us to double the tap length internally.

By redesigning the clock generation circuitry to use an oscillator at 20 Mhz, with a divide by 2 to generate a 10 Mhz clock, we can provide a 20 Mhz clock to the '256, and a 10 Mhz input sampling rate. This will also move the upper transition frequency away from the Nyquist sampling limit. Selecting the input sample rate to be 10 Mhz instead of 20 Mhz will allow us to double the number of taps available (per device).

Rerunning the filter design program and selecting 20 Mhz clock rate and "clk/2" as the input sample rate will provide us with 32 taps per device. Edit the <filename>.DSP file to show 128, and enter the following filter design criteria:

- Bandpass filter
- Frequency #2 = $0.378 * f_s$
- Frequency #1 = $0.338 * f_s$
- Free Parameter = transition width
- Filter order = 128
- Pass band ripple = 100 milli dB
- Stopband attenuation = -50 dB

Compiling this filter and re-iterating steps 10-13 listed initially will prove that 54 taps are required to implement this filter at the higher clock rates. Since the input sample rate is now 50% of the system clock rate, each device is capable of providing 32 taps. Only two '256 devices are now required to implement this function. Experimenting with the filter design program will show that a system clock equal to or greater than 16.5 Mhz will allow this function to be implemented (to full design specifications) using only 2 devices.



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